

*Patent Application*

*for:*

40-Gb/s CLOCK AND DATA RECOVERY CIRCUIT IN 0.18  $\mu\text{m}$  TECHNOLOGY

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CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority under 35 U.S.C. §119(e) to co-pending  
5 and commonly-assigned Provisional Application Serial No. 60/445,722, entitled  
“A 40-GB/S CLOCK AND DATA RECOVERY CIRCUIT IN 0.18 MM CMOS  
TECHNOLOGY,” filed on February 7, 2003, by Jri Lee and Behzad Razavi,  
attorney’s docket number 30448.116-US-P1, which application is incorporated by  
reference herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention.

The present invention relates generally to 40-Gb/s data, and in particular, to a 40-  
Gb/s clock and data recovery circuit in 0.18  $\mu$ m CMOS technology.

2. Description of the Related Art.

(Note: This application references a number of different publications as indicated  
throughout the specification by reference numbers enclosed in brackets, e.g., [x]. A list  
of these different publications ordered according to these reference numbers can be found  
20 below in the section entitled “References.” Each of these publications is incorporated by  
reference herein.)

Clock and data recovery (CDR) circuits operating at tens of gigabits per second  
pose difficult challenges with respect to speed, jitter, signal distribution, and power  
consumption. Half-rate 40-Gb/s CDR circuits have been implemented in bipolar  
25 technology [1,2], but they require 5 V supplies and draw 1.6 to 5 watts of power. (The  
work in [1] uses an external oscillator and 90° phase shifter.) On the other hand, the  
recent integration of 10-Gb/s receivers in CMOS technology [3] encourages further  
research on CMOS solutions for higher speeds, especially if it enables low-voltage, low-  
power realization. The present invention comprises a design and experimental  
30 verification of a 40-Gb/s phase-locked CDR circuit fabricated in 0.18- $\mu$ m CMOS  
technology.

## BRIEF SUMMARY OF THE INVENTION

A 40-Gb/s clock and data recovery (CDR) circuit incorporates a quarter-rate phase detector and a multi-phase voltage controlled oscillator to re-time and de-multiplex  
5 a 40-Gb/s input data signal into four 10-Gb/s output data signals. The circuit is fabricated in 0.18  $\mu\text{m}$  CMOS technology.

## BRIEF DESCRIPTION OF THE DRAWINGS

Referring now to the drawings in which like reference numbers represent  
10 corresponding parts throughout:

FIG. 1A is a block diagram that illustrates the architecture of a clock and data recovery (CDR) circuit of the preferred embodiment of the present invention;

FIG. 1B is a timing diagram that illustrates the operation of the clock and data recovery circuit in the preferred embodiment of the present invention;

15 FIG. 2A is a schematic that illustrates a half-quadrature voltage-controlled oscillator according to the preferred embodiment of the present invention;

FIG. 2B is a schematic that illustrates a modification of FIG. 2A;

FIG. 2C is a schematic realization of a  $-G_m$  cell according to the preferred embodiment of the present invention;

20 FIG. 3A is a schematic that illustrates a quarter-rate phase detector and voltage-to-current converter according to the preferred embodiment of the present invention;

FIG. 3B is a graph that illustrates the characteristic operation of the quarter-rate phase detector and voltage-to-current converter;

FIG. 4A depicts the master-slave flip-flop used in the phase detector according to  
25 the preferred embodiment of the present invention;

FIG. 4B depicts an XOR gate used in the phase detector according to the preferred embodiment of the present invention;

FIG. 5 is a micrograph that shows a photo of a die for the clock and data recovery circuit that has been fabricated in a 0.18  $\mu\text{m}$  CMOS technology;

30 FIG. 6A is a graph showing the tuning range of the voltage-controlled oscillator according to the preferred embodiment of the present invention;

FIG. 6B is a graph showing the free-running spectrum of the voltage-controlled oscillator according to the preferred embodiment of the present invention;

FIG. 7A is a graph that depicts the clock and data recovery circuit input and output waveforms under locked condition in response to a pseudo-random sequence of length  $2^{31}-1$ ; and

FIG. 7B is a graph that shows the recovered clock, suggesting an rms jitter of 1.756 ps and a peak-to-peak jitter of 9.67 ps.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following description, reference is made to the accompanying drawings which form a part hereof, and which is shown, by way of illustration, several embodiments of the present invention. It is understood that other embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.

##### A. Clock and Data Recovery (CDR) Architecture

FIG. 1A is a block diagram that illustrates the architecture of a clock and data recovery (CDR) circuit 10 according to the preferred embodiment of the present invention. The CDR circuit 10 includes: (1) a multi-phase voltage-controlled oscillator (VCO) 12 for accepting a control signal and for changing a frequency of a clock signal output from the VCO 12 in response thereto, wherein the VCO 12 outputs a plurality of phases of the clock signal; (2) a quarter-rate phase detector (PD) 14 for sampling an input data signal using the phases of the clock signal received from the VCO 12 and generating a plurality of data output signals in response thereto, wherein each of the data output signals detects an edge or transition in the input data signal and whether the edge is early or late with respect to its corresponding clock signal phase; (3) a Voltage-to-Current (V/I) Converter 16 for converting the data output signals from the phase detector 14 to a control current; and (4) a loop filter (LPF) 18 for integrating the control voltage from the V/I Converter 16 and for outputting the control signal to the VCO 12 in response thereto.

Specifically, the circuit 10 accepts a single 40-Gb/s input data signal  $D_{in}$ , and re-times and de-multiplexes the input data signal  $D_{in}$  into a plurality of 10-Gb/s output data

signals  $D1_{out}$ ,  $D2_{out}$ ,  $D3_{out}$  and  $D4_{out}$ . To accomplish this function, the PD 14 uses half-quadrature phases of the clock signal CK provided by the VCO 12 to sample the input data signal  $D_{in}$ , thereby detecting the edges or transitions in the data input signal  $D_{in}$  and determining whether the clock signal CK is early or late. Specifically, four 10-GHz  
5 phase offsets  $CK_0$ ,  $CK_{45}$ ,  $CK_{90}$  and  $CK_{135}$  of the clock signal are output from the VCO 12, wherein adjacent ones of the phase offsets  $CK_0$ ,  $CK_{45}$ ,  $CK_{90}$  and  $CK_{135}$  of the clock signal are half-quadrature phases, i.e., are offset in phase by  $45^\circ$  as indicated by their subscripts.

FIG. 1B is a timing diagram that illustrates the operation of the CDR circuit 10 in  
10 the preferred embodiment of the present invention. The PD 14 uses both the leading and trailing edges of the four 10-GHz phase offsets  $CK_0$ ,  $CK_{45}$ ,  $CK_{90}$  and  $CK_{135}$  of the clock signal provided by the VCO 12 to sample the input data signal  $D_{in}$  every 12.5 picoseconds (ps), in order to detect edges or transitions in the input data signal  $D_{in}$ , thereby re-timing and de-multiplexing the 40-Gb/s input data signal  $D_{in}$  into the four 10-  
15 Gb/s output data signals  $D1_{out}$ ,  $D2_{out}$ ,  $D3_{out}$  and  $D4_{out}$ . The PD 14 also determines whether the clock signal CK is early or late. Using this quarter-rate (10-Gb/s) sampling, flip-flops (not shown) in the PD 14 have a hold time that can be four times as long as that required at full-rate (40-Gb/s) operation, but their acquisition speed must still guarantee correct sampling of the input data signal  $D_{in}$  in less than 50 ps.

20 Note that, in the absence of edges or transitions in the input data signal  $D_{in}$ , the V/I Converter 16 generates no output current, leaving its control line to the LPF 18 and VCO 12 undisturbed. Note also that the circuit 10 is fully differential, except for the control line to the LPF 18 and VCO 12.

## 25 B. Components of the Clock and Data Recovery Circuit

### 1. Voltage-Controlled Oscillator

The speed, jitter, and driving capability required of the oscillator point to the use of an LC realization. A number of multi-phase LC oscillators have been reported. Coupled oscillators [4,5] operate away from the resonance frequency of the tanks so as to  
30 create the required phase shift, thus bearing a trade-off between reliability of oscillation and the phase noise [5]. Furthermore, such topologies are prone to oscillation at more

than one frequency because they can satisfy gain and phase requirements at multiple frequencies. The multi-phase oscillator in [6] drives transmission lines by a gain stage loaded by resistors, incurring energy loss in each cycle.

FIG. 2A is a schematic that illustrates a half-quadrature VCO 12 according to the preferred embodiment of the present invention, FIG. 2B is a schematic that illustrates a modification of FIG. 2A, and FIG. 2C is a schematic realization of a  $-G_m$  cell according to the preferred embodiment of the present invention.

The multi-phase VCO 12 introduced here is based on the concept of differential stimulus of a closed-loop transmission line at equally-spaced points. As illustrated in FIG. 2A, the loop circuit of the VCO 12 sustains a phase separation of  $180^\circ$  at diagonally-opposite nodes, providing  $45^\circ$  phase steps in between for the clock signal, wherein the nodes are labeled as  $0^\circ$ ,  $45^\circ$ ,  $90^\circ$ ,  $135^\circ$ ,  $180^\circ$ ,  $225^\circ$ ,  $270^\circ$  and  $315^\circ$ . Unlike the topologies in [5] and [7], this circuit does not operate away from the resonance frequency.

Moreover, the VCO 12 oscillation frequency is uniquely given by the travel time of the wave around the loop. Also, in contrast to the design in [6], the transmission line requires no termination resistors, thereby displaying lower phase noise and larger voltage swings for a given power dissipation and inductor  $Q$ .

The topology of FIG. 2A nonetheless necessitates long interconnects between the nodes and their corresponding  $-G_m$  cells. However, recognizing that diagonally-opposite inductors  $L_1$ ,  $L_2$ ,  $L_3$ ,  $L_4$ ,  $L_5$ ,  $L_6$ ,  $L_7$  and  $L_8$  carry currents that are  $180^\circ$  out of phase, the circuit can be modified as shown in FIG. 2B, wherein inductor elements of the VCO 12 are grouped into differential structures  $L_1/L_5$ ,  $L_2/L_6$ ,  $L_3/L_7$  and  $L_4/L_8$ , and  $-G_m$  cells are placed in close proximity to the nodes of the VCO 12.

Exploiting the higher  $Q$  of differential inductors [8], the VCO 12 uses a structure for the  $-G_m$  cell as shown in FIG. 2C, thereby shaping the rising and falling edges by the PMOS transistors  $M_1$ ,  $M_2$ ,  $M_3$  and  $M_4$ , and hence lowering the up-conversion of  $1/f$  noise [9]. SpectreRF™ simulations indicate that, for a given power dissipation, inductor  $Q$ , and frequency of oscillation, the proposed VCO 12 achieves twice the voltage swings and 12 dB lower phase noise than that in [6].

Using the structure of the  $-G_m$  cell shown in FIG. 2C, each differential port of the VCO 12 is buffered by an inductively-loaded differential pair of switches  $M_1$ - $M_3$  and  $M_2$ -

M<sub>4</sub>. These buffers performing the following: (1) isolate the VCO 12 from the long interconnects to the PD 14 that would otherwise introduce greater uncertainty in the oscillation frequency; (2) generate voltage swings above the supply voltage, thus driving the flip-flops of the PD 14 efficiently; and (3) isolate the VCO 12 from the edges or  
5 transitions coupled through the PD 14.

## 2. Phase Detector

FIG. 3A is a schematic that illustrates a quarter-rate PD 14 and V/I Converter 16 according to the preferred embodiment of the present invention, and FIG. 3B is a graph  
10 that illustrates the characteristic operation thereof. The PD 14 employs eight flip-flops 20 that sample the input data signal  $D_{in}$  at 12.5-ps intervals based on the clock signal from the VCO 12 using the phase offsets  $CK_0$ ,  $CK_{45}$ ,  $CK_{90}$ , and  $CK_{135}$ , wherein  $CK_{180} = \overline{CK_0}$ ,  $CK_{225} = \overline{CK_{45}}$ ,  $CK_{270} = \overline{CK_{90}}$  and  $CK_{315} = \overline{CK_{135}}$ . The PD 14 also employs eight XOR  
15 gates 22 that compare the outputs from adjacent or consecutive flip-flops 20. The V/I Converter 16 employs four Level Converters (LE) 24 that generate a current level from the combined output of the XOR gates 22 as the control line to the LPF 18 and VCO 12.

In a manner similar to an Alexander topology [10], the PD 14 compares every two adjacent or consecutive samples stored by the adjacent or consecutive flip-flops 20 by means of the associated XOR gate 22, which generates a net output current if the two  
20 adjacent or consecutive samples are unequal, thereby indicating that an edge or transition has occurred in the input data signal  $D_{in}$ . When no edges or transitions occur, the flip-flops 20 storing the two adjacent or consecutive samples produce equal outputs, the XOR gate 22 outputs a zero, and the control line from the V/I Converter 16 has a zero current.

The early-late phase detection method used herein exhibits a bang-bang  
25 characteristic, forcing the CDR circuit 10 to align every other edge of the clock signal CK with the zero crossings of the input data signal  $D_{in}$  under the locked condition. In reality, the meta-stable behavior of the flip-flops 20 leads to a finite PD 14 gain, allowing the clock signal CK edges to sustain some offset with respect to the zero crossings of the input data signal  $D_{in}$ .

30 Shown in FIG. 3B is the input/output characteristic of the PD 14 together with the V/I Converter 16, obtained by transistor-level simulations while the circuit 10 senses a

40-Gb/s random stream of the input data signal  $D_{in}$  and eight phases of the 10-GHz clock signal CK. For a phase error less than  $\pm 2.5$  ps, the PD 14 displays a relatively constant gain of 100  $\mu\text{A}/\text{ps}$ .

Even though the flip-flops 20 of the PD 14 operate with a 10-GHz clock signal CK, proper sampling of the 40-Gb/s input data signal  $D_{in}$  still requires fast recovery from the previous state and rapid acquisition of the present input. To this end, both a wide sampling bandwidth and a short clock signal CK transition time are necessary.

FIG. 4A is a schematic of the master-slave flip-flop 20 used in the PD 14 according to the preferred embodiment of the present invention. The master-slave flip-flop 20 includes switches  $M_1$ - $M_{13}$  and  $M_b$  and capacitors  $C_1$ - $C_2$ . The flip-flop 20 latches input data signal  $D_{in}$ , using a CK clock signal provided from the VCO 12 buffer, and data output signals  $D_{out}$ .

NMOS switches  $M_1$  and  $M_2$  sample the input data signal  $D_{in}$  on the parasitic capacitances at nodes X and Y when CK is high. Since the minimum input common-mode (CM) level is dictated by the gate-source voltage of  $M_3$ - $M_4$  and the headroom required by  $I_{SS}$ , the sampling switches  $M_1$  and  $M_2$  experience only an overdrive voltage of 0.5 V even if CK reaches  $V_{DD}$ , failing to provide fast sampling. This issue is remedied by setting the CM level of CK and CK equal to  $V_{DD}$ , a choice afforded by the inductively-loaded stages of the VCO 12 buffer. The peak value of CK thus exceeds  $V_{DD}$  by 0.8 V, more than doubling the sampling speed of  $M_1$  and  $M_2$ . The large clock swings also minimize the transition times.

With large clock swings available, the current switching in pairs  $M_5$ - $M_6$ ,  $M_7$ - $M_8$  and  $M_9$ - $M_{10}$  is accomplished by gate control rather than conventional source-coupled steering. The proposed topology offers two advantages: (1) since the tail current source is removed,  $M_{11}$ - $M_{13}$  can be quite narrower, presenting a smaller capacitance to the VCO 12 buffer; (2) since the drain currents of  $M_{11}$ - $M_{13}$  are not limited by a tail current source, these transistors experience “class AB” switching, drawing a large current at the peak of the clock swing and providing greater voltage swings and a higher gain in the data path.

FIG. 4B is a schematic of the XOR gate 22 used in the PD, along with the V/I Converter 16 (i.e., the Level Converter 24), according to the preferred embodiment of the present invention. The XOR gate 22 accepts signals a and b as input and includes



switches  $M_1$ - $M_3$ , while the V/I Converter 16 accepts the output of the XOR gate 22 (as well as the next XOR gate 22) as input and includes switches  $M_4$ - $M_7$ . The V/I Converter 16 outputs the control line  $V_{out}$  to the LPF 18 (and then to the VCO 12).

The XOR gates 22 used in the PD 14 must exhibit symmetry with respect to their two inputs and operate with a low supply voltage. The XOR gate 22 shown in FIG. 4B is a modified version of that in [11], with transistors  $M_2$  and  $M_3$  forming local positive feedback loops and avoiding the reference voltage necessary in the realization in [11]. The V/I Converter 16 copies the output current of the XOR gate 22, providing nearly rail-to-rail swings for the control line  $V_{out}$  to the LPF 18 (and VCO 12).

### C. Experimental Results

The CDR circuit 10 of the present invention has been fabricated in a 0.18  $\mu\text{m}$  CMOS technology. FIG. 5 is a micrograph that shows a photo of the die, which measures  $1.0 \times 1.4 \text{ mm}^2$ . The circuit is tested on a high-speed probe station with a 40-Gb/s Anritsu<sup>TM</sup> random data generator providing the input.

Shown in FIG. 6A is the VCO 12 tuning range and shown in FIG. 6B is the free-running spectrum. The VCO 12 provides a tuning range of 1.2-GHz with a free-running phase noise of -105 dBc/Hz at 1-MHz offset.

FIG. 7A depicts the CDR circuit 10 input and output waveforms under locked condition in response to a pseudo-random sequence of length  $2^{31}-1$ . The de-multiplexed data experiences some inter-symbol interference (ISI), but if further de-multiplexing is included on the same chip, the ISI can be tolerated. FIG. 7B shows the recovered clock, suggesting an rms jitter of 1.756 ps and a peak-to-peak jitter of 9.67 ps.

However, as shown in the inset, the oscilloscope itself suffers from rms and peak-to-peak jitters of 1.508 ps and 8.89 ps, respectively. Thus, the CDR circuit 10 output contains a jitter of 0.9 ps,rms and at most 9.67 ps,pp. (It is unclear whether and how the peak-to-peak values can be subtracted.)

The performance of this work and some other previously-published CDR circuits is summarized in Table 1. (The power dissipation noted here for the design in [2] excludes their limiting amplifier and frequency detector contribution and was obtained through private communication with M. Reinhold.)

	Reference [1]	Reference [2]	Reference [6]	Present Invention
Input Data Rate	40-Gb/s	40-Gb/s	10-Gb/s	40-Gb/s
Output Data Rate	2 x 20-Gb/s	4 x 10-Gb/s	2 x 5-Gb/s	4 x 10-Gb/s
Rec. Clock Jitter	0.8 ps,rms	0.7 ps,rms	1.2 ps,rms	0.9 ps,rms
Power Dissipation	1.6 W	4.3 W	360 mW	144 mW
Supply Voltage	5 V	5 V	1.8 V	2 V
Area	0.9 mm x 0.9 mm	3 mm x 3 mm	1.9 mm x 1.5 mm	1.0 mm x 1.4 mm
Technology	50-GHz Bipolar (uses external VCO and divider)	72-GHz SiGe	0.18- $\mu$ m CMOS	0.18- $\mu$ m CMOS

### References

The following references are incorporated by reference herein:

- 5 [1] M. Wurzer et al, "A 40-Gb/s Integrated Clock and Data Recovery Circuit in a 50-GHz  $f_T$  Silicon Bipolar Technology," IEEE Journal of Solid-State Circuits, vol. 34, pp. 1320-1324, Sept. 1999.

- [2] M. Reinhold et al, "A Fully Integrated 40-Gb/s Clock and Data Recovery IC with 1:4 DEMUX in SiGe technology," IEEE Journal of Solid-State Circuits, vol. 36, pp. 10 1937-1945, Dec. 2001.

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- 15 [5] T. P. Liu, "A 6.5-GHz Monolithic CMOS Voltage-Controlled Oscillator," ISSCC Dig. of Tech. Papers, pp. 404-405, Feb. 1999.

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[8] M. Danesh et al., "A Q-Factor Enhancement Technique for MMIC Inductors," Proc. IEEE Radio Frequency Integrated Circuits Symp., pp. 217–220, April 1998.

[9] A. Hajimiri and T. H. Lee, "A General Theory of Phase Noise in Electrical Oscillators," IEEE Journal of Solid-State Circuits, pp. 179-194, Feb. 1998.

5 [10] J. D. H. Alexander, "Clock Recovery from Random Binary Data," Electronics Letters, vol. 11, pp. 541-542, Oct. 1975.

[11] B. Razavi et al, "Design Techniques for Low-Voltage High-Speed Digital Bipolar Circuits," IEEE Journal of Solid-State Circuits, pp. 332-9, March 1994.

10 Conclusion

This concludes the description of the preferred embodiment of the invention. The following describes some alternative embodiments for accomplishing the present invention.

For example, the present invention could be used with many types of circuits, and  
15 not just those described herein. Moreover, any number of different components or different configurations of components could be used without departing from the scope of the present invention. Finally, any number of input data signals, phase offset clock signals and de-multiplexed output data signals could be generated by the present invention.

20 The foregoing description of one or more embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims  
25 appended hereto.